

EXHIBIT B

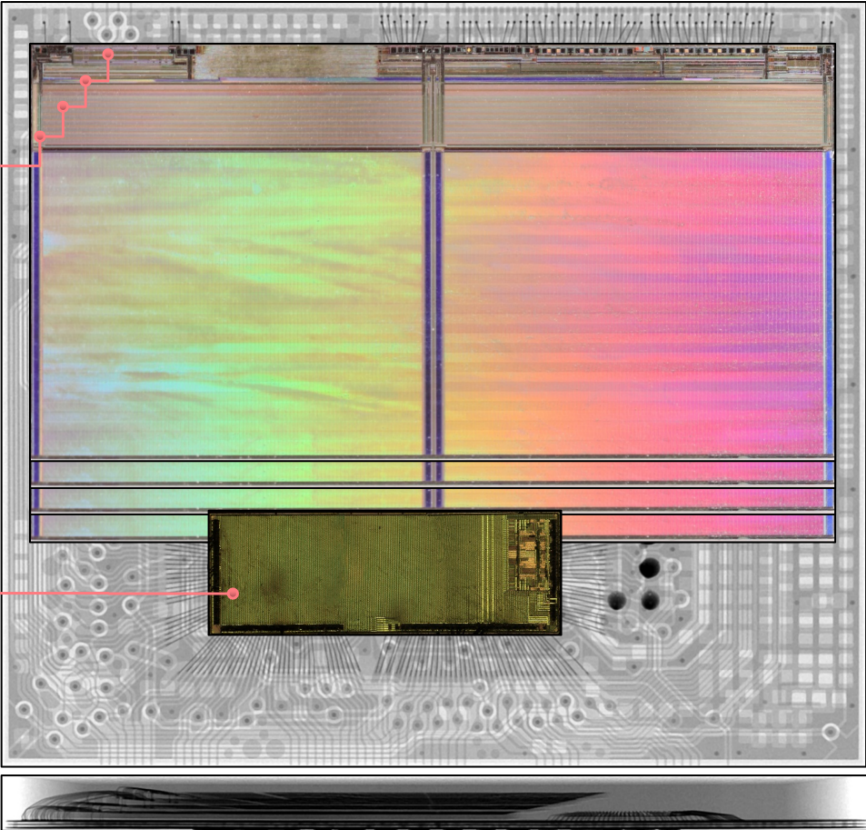
U.S. Patent No. 6,724,241 (“’241 Patent”)

Accused Products

Samsung products with SanDisk/Toshiba 64L 3D NAND flash chips, including without limitation the Samsung Galaxy S10 (“Accused Products”), infringe at least Claims 1-3, 6-8, and 11 of the ’241 Patent.

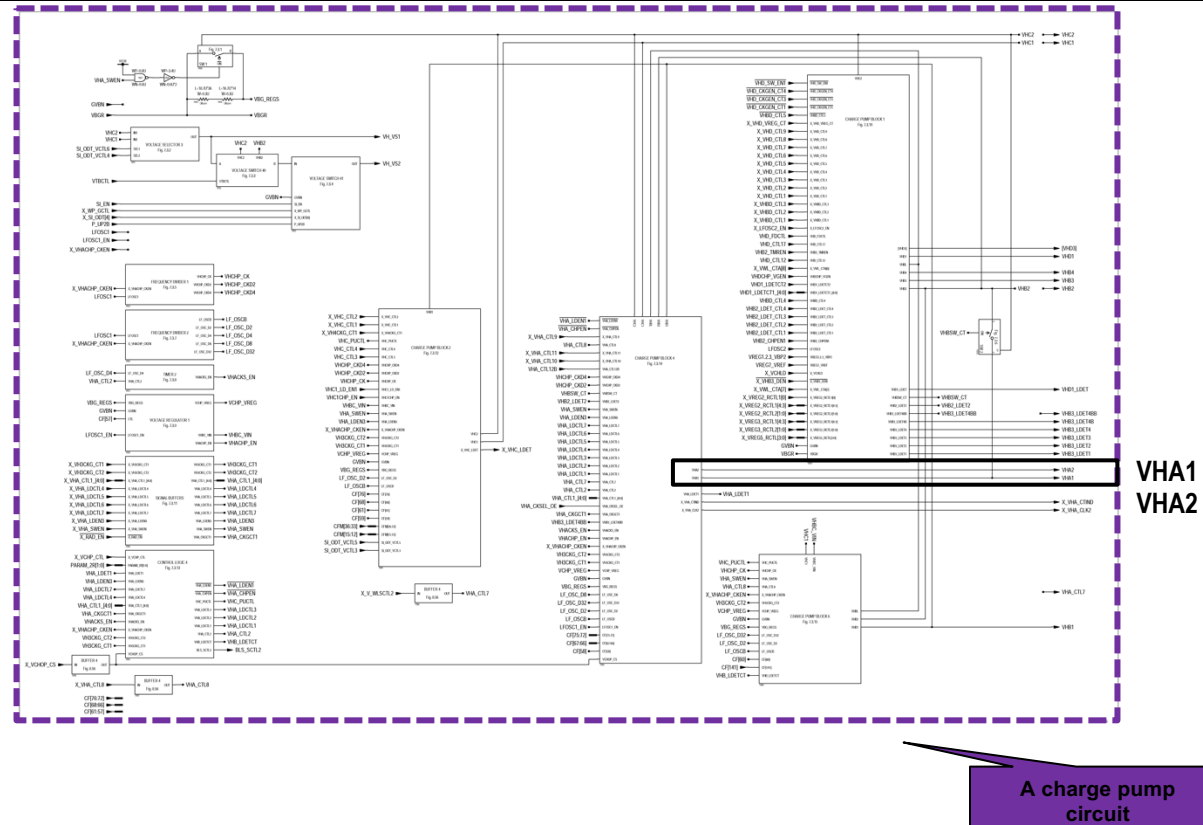
Claim 1

Claim 1	Accused Product
[1pre] 1. A charge pump circuit for generating a charge pump voltage having minimal voltage ripples, comprising:	<p>To the extent the preamble is limiting, each Accused Product includes a charge pump circuit for generating a charge pump voltage having minimal voltage ripples.</p> <p>For example, the Samsung Galaxy S10 includes the charge pump circuit of the SanDisk/Toshiba 3D NAND flash chip, die identifier FRN1256G.</p> <p><i>See, e.g.:</i></p>

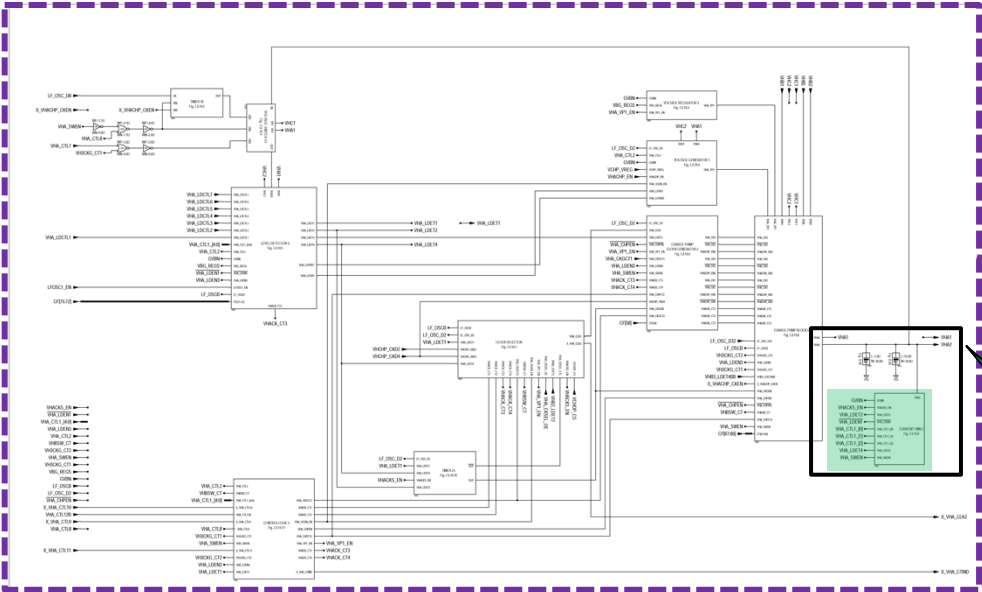
Claim 1	Accused Product
	<div data-bbox="646 267 1012 362"><p>3 - Toshiba #THGAF8T0T43BAIR Multichip Memory - 128 GB 3D TLC NAND Flash, Memory Controller (5-Die Pkg.) Pkg Size: 13 x 11.5 mm</p></div> <div data-bbox="735 391 1012 470"><p>3.1 - Toshiba #FRN1256G 3D TLC NAND Flash Memory - 32 GB Die Size: 12.18 x 6.27 mm</p></div> <div data-bbox="835 816 1012 896"><p>3.2 - Toshiba #FRZ8 0002 Memory Controller Die Size: 5.2 x 1.8 mm</p></div> <div data-bbox="653 1040 835 1084"><p>Function: Memory: Non-Volatile</p></div> <div data-bbox="1022 267 1883 1092"></div> <div data-bbox="636 1101 1829 1138"><p>Source: TechInsights Deep Dive Teardown, Samsung Galaxy S10 SM-G9730 ID339612-RZe</p></div>

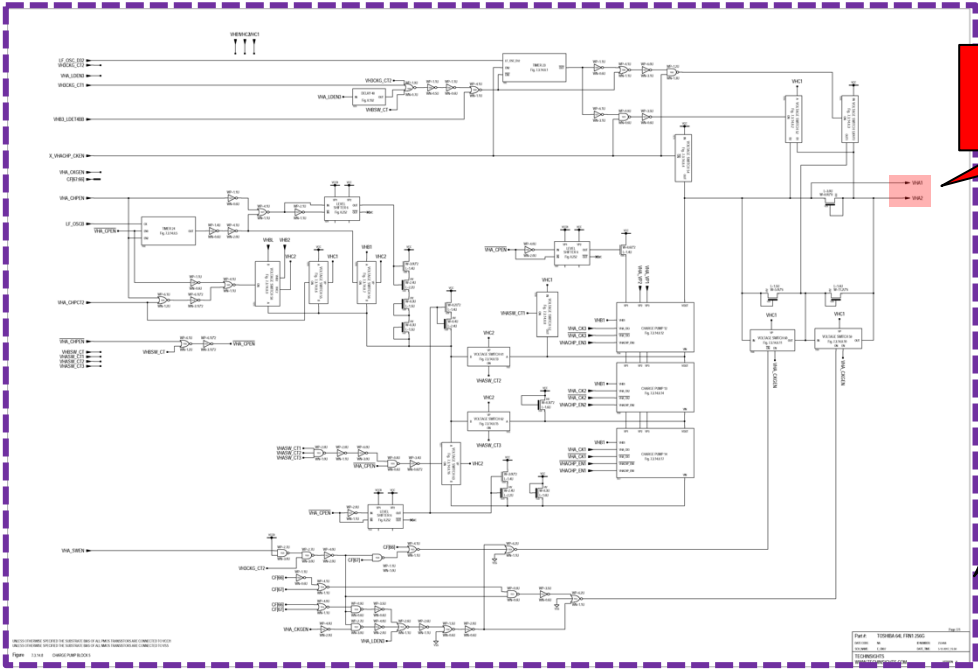
Claim 1

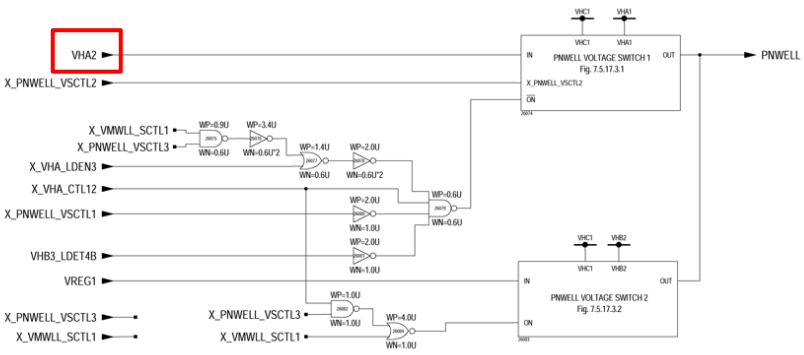
Accused Product

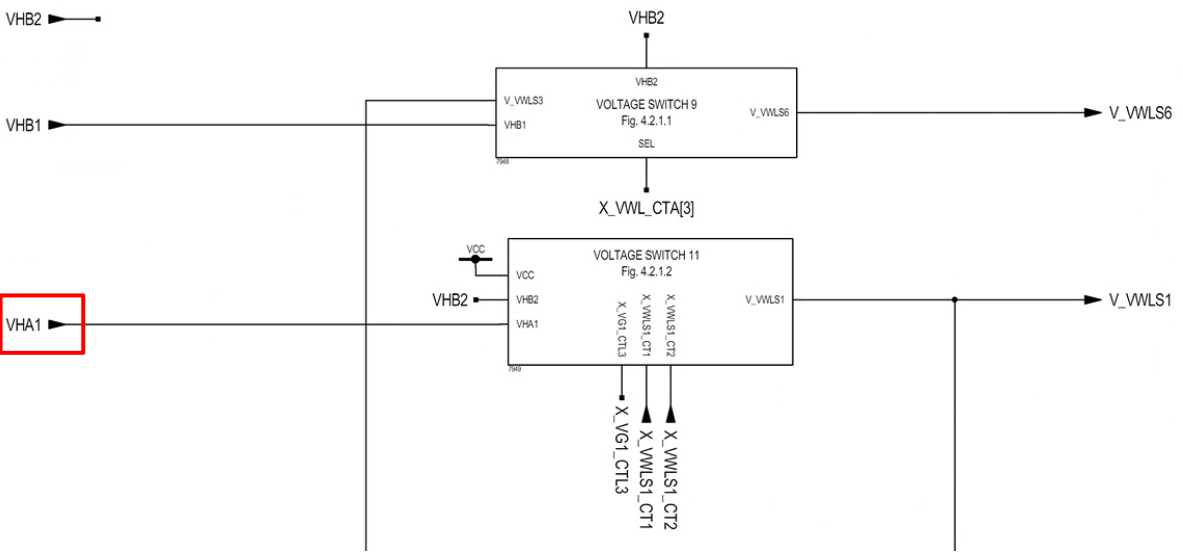


Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3 Charge Pump System

Claim 1	Accused Product
	<div data-bbox="630 264 1606 852"></div> <p data-bbox="630 917 1827 990">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3 Charge Pump System</p>

Claim 1	Accused Product
	<div data-bbox="640 264 1612 930"></div> <div data-bbox="1591 305 1871 412" style="background-color: red; color: black; padding: 5px;"><p>for generating a charge pump voltage (VHA1, VHA2)</p></div> <div data-bbox="1623 483 1843 574" style="background-color: white; border: 1px solid black; padding: 5px;"><p>VHA1 and VHA2 are driven by the same pumping circuit</p></div> <div data-bbox="1629 646 1839 716" style="background-color: purple; color: white; padding: 5px;"><p>A charge pump circuit</p></div> <p data-bbox="632 992 1829 1062">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5</p>

Claim 1	Accused Product
	<p data-bbox="688 272 1255 332">Charge pump output voltage VHA2 is provided to high voltage switches to selectively drive PNWELL.</p>  <p data-bbox="634 776 1831 844">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.5.17.3 PNWELL Voltage Selector</p>

Claim 1	Accused Product
	<p>Charge pump output voltage VHA1 is provided to high voltage switches to selectively drive wordline circuits.</p>  <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 4.2.1 Wordline Voltage Switch Block 1</p>
<p>1[a] a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages;</p>	<p>Each Accused Product includes a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages.</p> <p>For example, in the pumping circuit, 1, 2, or 3 main stages can be enabled for operation. Supply voltage can be selected from external VCC or internally generated pumped voltages VHBL or VHB1. VHA2 is provided to a level detector which suspends pump clocks when a desired level is reached. VHA2 is scaled by a fixed ratio voltage divider (Voltage Divider 2). It is then compared (using Amplifier 12) to an adjustable reference voltage (generated by Reference Voltage Regulator). A 4-bit digital code CF(75:72) adjusts the output reference voltage by shorting out</p>

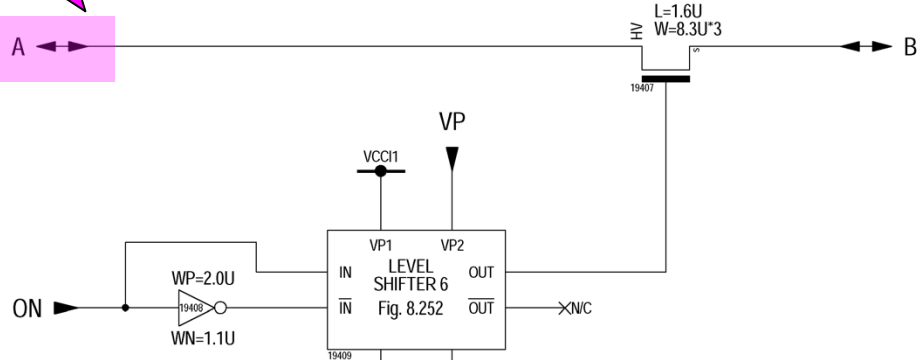
Claim 1	Accused Product
	<p>resistors in a resistor divider, thereby providing programmable pump output voltage levels on VHA1 and VHA2. A comparator (Amplifier 12) compares the scaled VHA2 to the programmable reference voltage. If the scaled VHA2 exceeds the programmable reference voltage, output VHA_LDET3 transitions from 1 to 0 to stop further pumping. VHA_CK2 and VHA_CK2* drive the middle stage of the pumping circuit. VHA_PH2 non-overlapping clocks drive Charge Pump 13. When VHA_PH2 clocks are suspended the pump stops operating so that VHA1 is limited to the voltage set by the level detector.</p> <p><i>See, e.g.:</i></p>

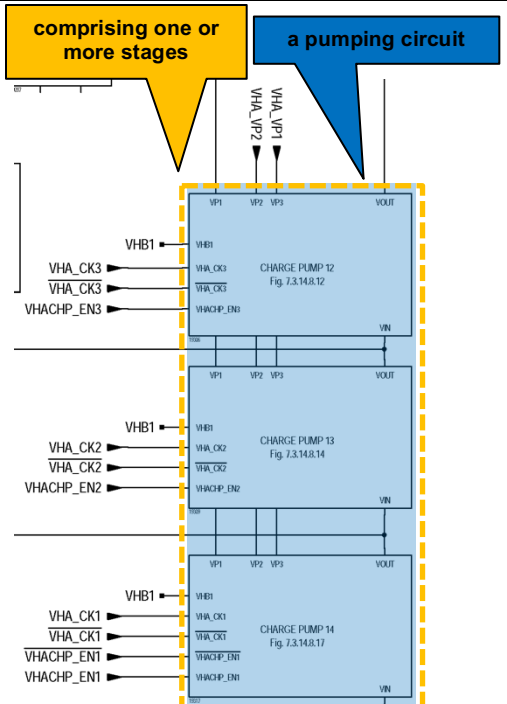
Claim 1

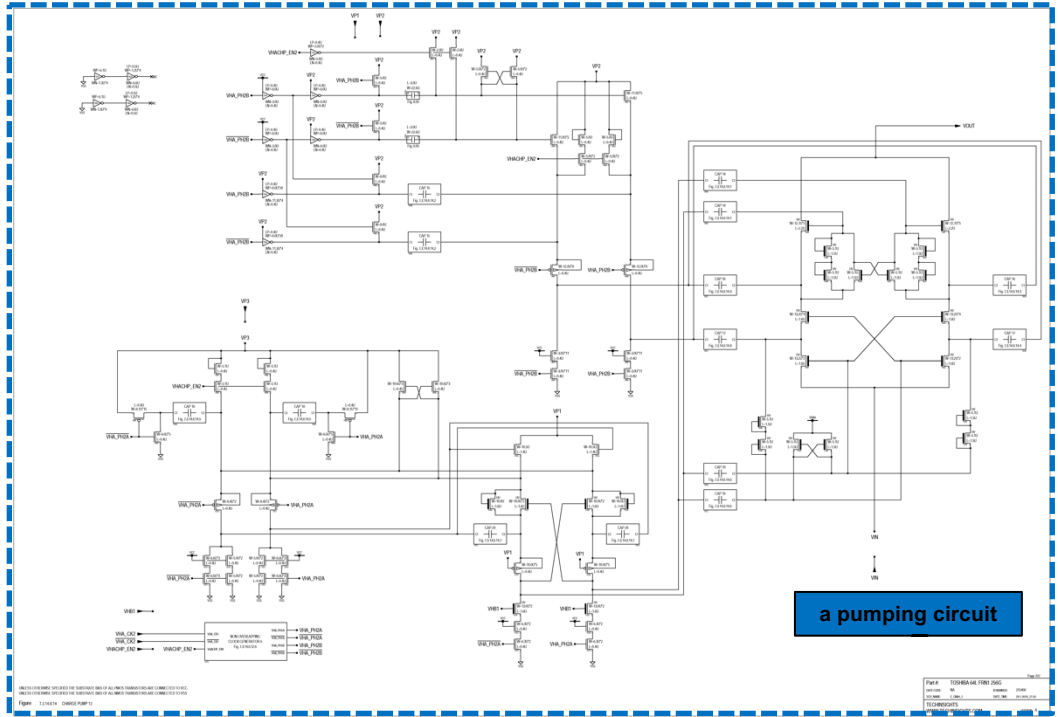
operable to receive a supply voltage

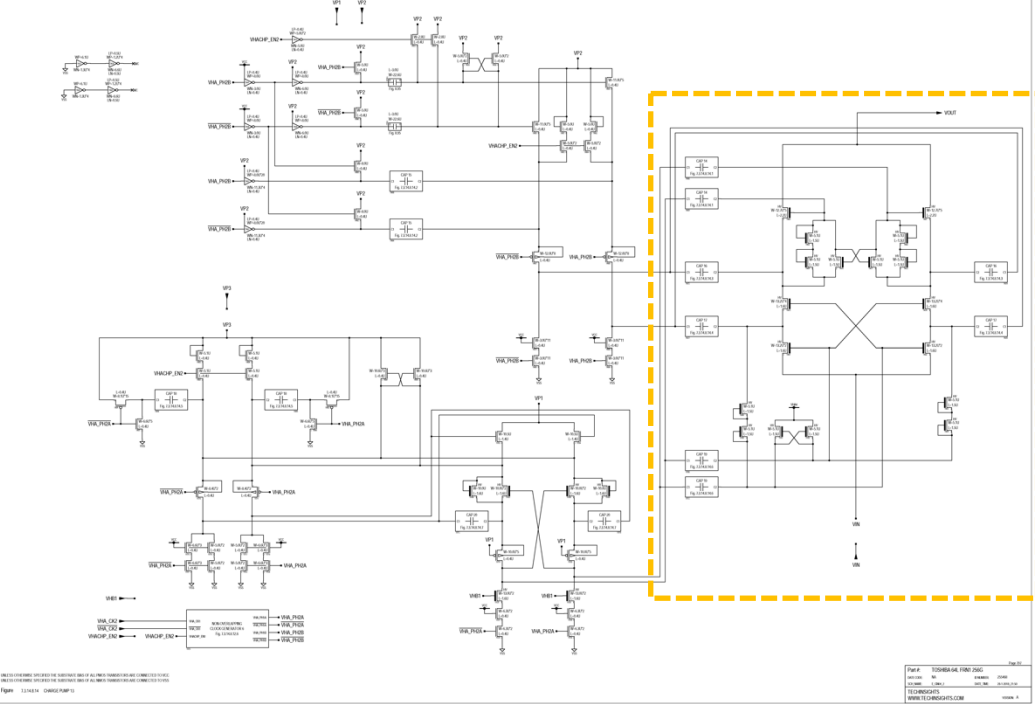
a pumping circuit

Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5

Claim 1	Accused Product
	<p data-bbox="632 264 966 329">operable to receive a supply voltage (VCC)</p>  <p data-bbox="632 808 1829 881">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.6 Voltage Switch 55</p>

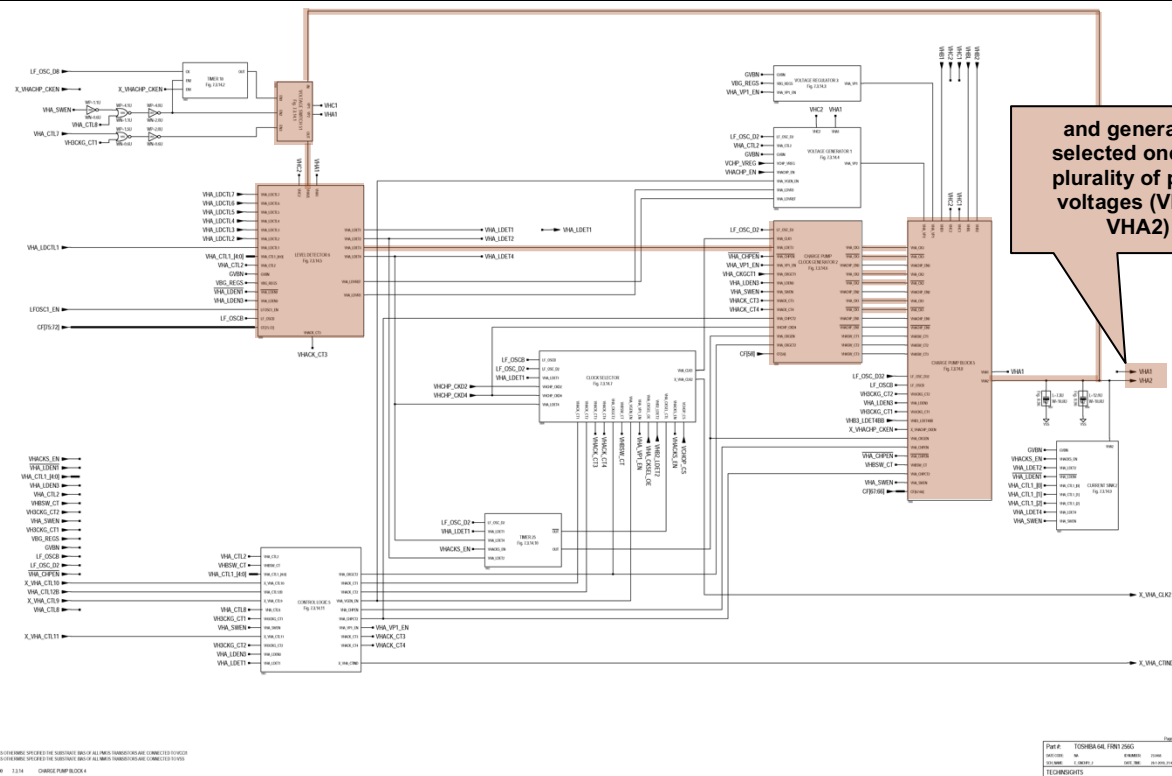
Claim 1	Accused Product
	 <p>The diagram illustrates a multi-stage charge pump circuit. It consists of three identical stages, labeled CHARGE PUMP 12, CHARGE PUMP 13, and CHARGE PUMP 14. Each stage has four inputs: VHB1, VHA_CK3, VHA_CK3, and VHACHP_EN3 (for Pump 12); VHB1, VHA_CK2, VHA_CK2, and VHACHP_EN2 (for Pump 13); and VHB1, VHA_CK1, VHA_CK1, and VHACHP_EN1 (for Pump 14). Each stage also has four outputs: VP1, VP2, VP3, and VOUT. The stages are connected in series, with the output of one stage serving as the input for the next. The entire block is enclosed in a dashed yellow border. Callouts indicate that the block 'comprising one or more stages' and 'a pumping circuit'.</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5</p>

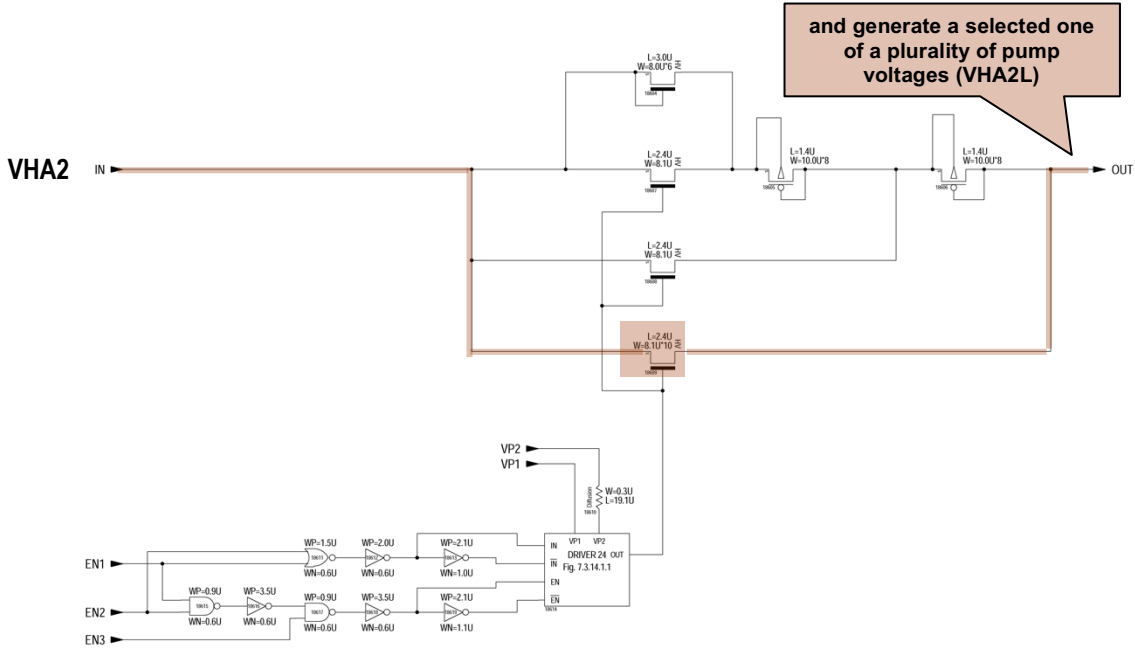
<p>Claim 1</p>	<p>Accused Product</p>
	 <p>The diagram illustrates a 3D NAND Charge Pump 13, a critical component for programming and erasing data in 3D NAND flash memory. It features a complex arrangement of transistors (labeled with part numbers like 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7, 1A8, 1A9, 1A10, 1A11, 1A12, 1A13, 1A14, 1A15, 1A16, 1A17, 1A18, 1A19, 1A20, 1A21, 1A22, 1A23, 1A24, 1A25, 1A26, 1A27, 1A28, 1A29, 1A30, 1A31, 1A32, 1A33, 1A34, 1A35, 1A36, 1A37, 1A38, 1A39, 1A40, 1A41, 1A42, 1A43, 1A44, 1A45, 1A46, 1A47, 1A48, 1A49, 1A50, 1A51, 1A52, 1A53, 1A54, 1A55, 1A56, 1A57, 1A58, 1A59, 1A60, 1A61, 1A62, 1A63, 1A64, 1A65, 1A66, 1A67, 1A68, 1A69, 1A70, 1A71, 1A72, 1A73, 1A74, 1A75, 1A76, 1A77, 1A78, 1A79, 1A80, 1A81, 1A82, 1A83, 1A84, 1A85, 1A86, 1A87, 1A88, 1A89, 1A90, 1A91, 1A92, 1A93, 1A94, 1A95, 1A96, 1A97, 1A98, 1A99, 1A100, 1A101, 1A102, 1A103, 1A104, 1A105, 1A106, 1A107, 1A108, 1A109, 1A110, 1A111, 1A112, 1A113, 1A114, 1A115, 1A116, 1A117, 1A118, 1A119, 1A120, 1A121, 1A122, 1A123, 1A124, 1A125, 1A126, 1A127, 1A128, 1A129, 1A130, 1A131, 1A132, 1A133, 1A134, 1A135, 1A136, 1A137, 1A138, 1A139, 1A140, 1A141, 1A142, 1A143, 1A144, 1A145, 1A146, 1A147, 1A148, 1A149, 1A150, 1A151, 1A152, 1A153, 1A154, 1A155, 1A156, 1A157, 1A158, 1A159, 1A160, 1A161, 1A162, 1A163, 1A164, 1A165, 1A166, 1A167, 1A168, 1A169, 1A170, 1A171, 1A172, 1A173, 1A174, 1A175, 1A176, 1A177, 1A178, 1A179, 1A180, 1A181, 1A182, 1A183, 1A184, 1A185, 1A186, 1A187, 1A188, 1A189, 1A190, 1A191, 1A192, 1A193, 1A194, 1A195, 1A196, 1A197, 1A198, 1A199, 1A200, 1A201, 1A202, 1A203, 1A204, 1A205, 1A206, 1A207, 1A208, 1A209, 1A210, 1A211, 1A212, 1A213, 1A214, 1A215, 1A216, 1A217, 1A218, 1A219, 1A220, 1A221, 1A222, 1A223, 1A224, 1A225, 1A226, 1A227, 1A228, 1A229, 1A230, 1A231, 1A232, 1A233, 1A234, 1A235, 1A236, 1A237, 1A238, 1A239, 1A240, 1A241, 1A242, 1A243, 1A244, 1A245, 1A246, 1A247, 1A248, 1A249, 1A250, 1A251, 1A252, 1A253, 1A254, 1A255, 1A256, 1A257, 1A258, 1A259, 1A260, 1A261, 1A262, 1A263, 1A264, 1A265, 1A266, 1A267, 1A268, 1A269, 1A270, 1A271, 1A272, 1A273, 1A274, 1A275, 1A276, 1A277, 1A278, 1A279, 1A280, 1A281, 1A282, 1A283, 1A284, 1A285, 1A286, 1A287, 1A288, 1A289, 1A290, 1A291, 1A292, 1A293, 1A294, 1A295, 1A296, 1A297, 1A298, 1A299, 1A300, 1A301, 1A302, 1A303, 1A304, 1A305, 1A306, 1A307, 1A308, 1A309, 1A310, 1A311, 1A312, 1A313, 1A314, 1A315, 1A316, 1A317, 1A318, 1A319, 1A320, 1A321, 1A322, 1A323, 1A324, 1A325, 1A326, 1A327, 1A328, 1A329, 1A330, 1A331, 1A332, 1A333, 1A334, 1A335, 1A336, 1A337, 1A338, 1A339, 1A340, 1A341, 1A342, 1A343, 1A344, 1A345, 1A346, 1A347, 1A348, 1A349, 1A350, 1A351, 1A352, 1A353, 1A354, 1A355, 1A356, 1A357, 1A358, 1A359, 1A360, 1A361, 1A362, 1A363, 1A364, 1A365, 1A366, 1A367, 1A368, 1A369, 1A370, 1A371, 1A372, 1A373, 1A374, 1A375, 1A376, 1A377, 1A378, 1A379, 1A380, 1A381, 1A382, 1A383, 1A384, 1A385, 1A386, 1A387, 1A388, 1A389, 1A390, 1A391, 1A392, 1A393, 1A394, 1A395, 1A396, 1A397, 1A398, 1A399, 1A400, 1A401, 1A402, 1A403, 1A404, 1A405, 1A406, 1A407, 1A408, 1A409, 1A410, 1A411, 1A412, 1A413, 1A414, 1A415, 1A416, 1A417, 1A418, 1A419, 1A420, 1A421, 1A422, 1A423, 1A424, 1A425, 1A426, 1A427, 1A428, 1A429, 1A430, 1A431, 1A432, 1A433, 1A434, 1A435, 1A436, 1A437, 1A438, 1A439, 1A440, 1A441, 1A442, 1A443, 1A444, 1A445, 1A446, 1A447, 1A448, 1A449, 1A450, 1A451, 1A452, 1A453, 1A454, 1A455, 1A456, 1A457, 1A458, 1A459, 1A460, 1A461, 1A462, 1A463, 1A464, 1A465, 1A466, 1A467, 1A468, 1A469, 1A470, 1A471, 1A472, 1A473, 1A474, 1A475, 1A476, 1A477, 1A478, 1A479, 1A480, 1A481, 1A482, 1A483, 1A484, 1A485, 1A486, 1A487, 1A488, 1A489, 1A490, 1A491, 1A492, 1A493, 1A494, 1A495, 1A496, 1A497, 1A498, 1A499, 1A500, 1A501, 1A502, 1A503, 1A504, 1A505, 1A506, 1A507, 1A508, 1A509, 1A510, 1A511, 1A512, 1A513, 1A514, 1A515, 1A516, 1A517, 1A518, 1A519, 1A520, 1A521, 1A522, 1A523, 1A524, 1A525, 1A526, 1A527, 1A528, 1A529, 1A530, 1A531, 1A532, 1A533, 1A534, 1A535, 1A536, 1A537, 1A538, 1A539, 1A540, 1A541, 1A542, 1A543, 1A544, 1A545, 1A546, 1A547, 1A548, 1A549, 1A550, 1A551, 1A552, 1A553, 1A554, 1A555, 1A556, 1A557, 1A558, 1A559, 1A560, 1A561, 1A562, 1A563, 1A564, 1</p>

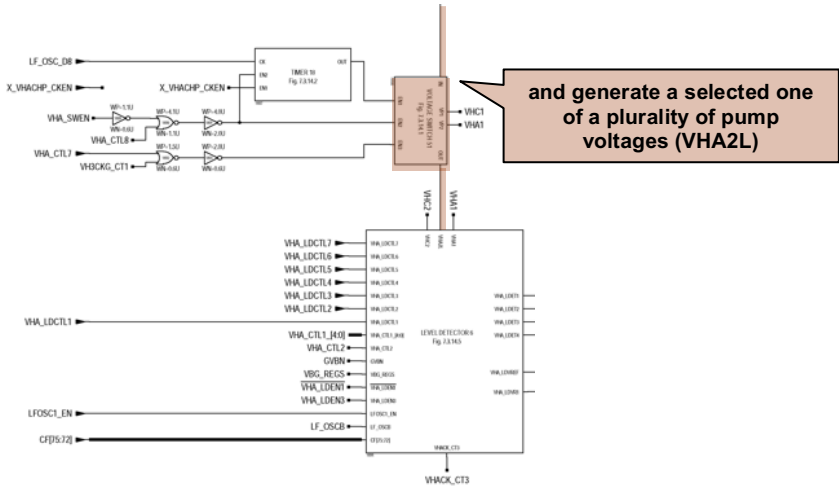
Claim 1	Accused Product
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>

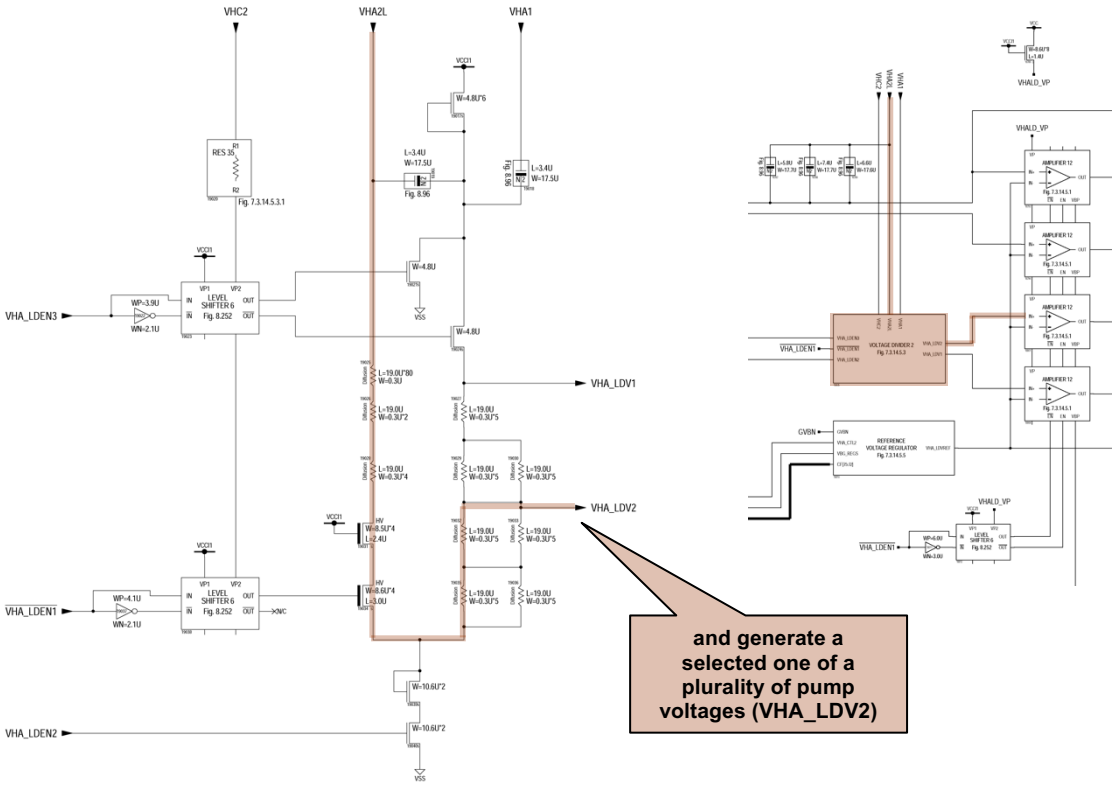
Claim 1

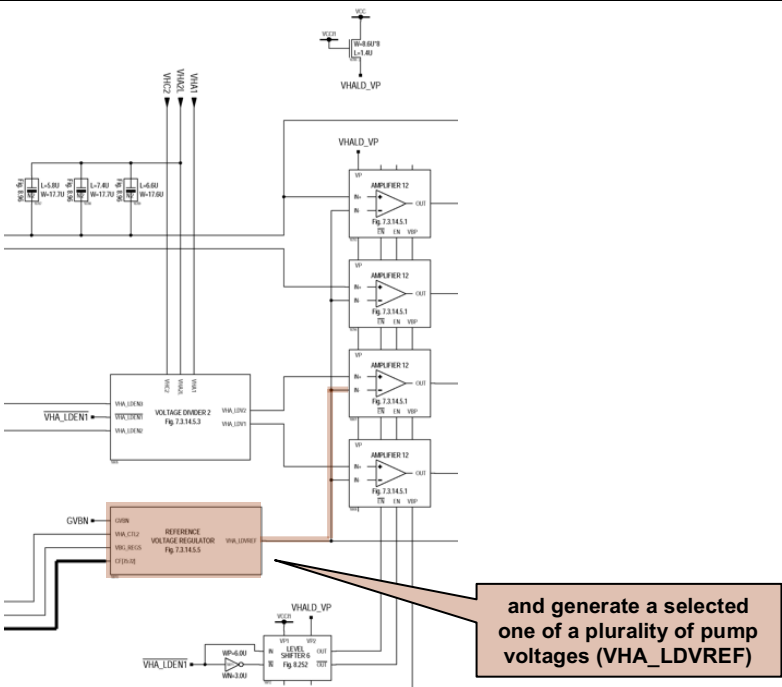
Accused Product



Claim 1	Accused Product
	 <p>The diagram shows a circuit for a voltage switch (VHA2). It includes an input terminal 'VHA2 IN' and an output terminal 'OUT'. The circuit features several transistors with specific dimensions (L, W) and a network of resistors. A callout box with a speech bubble shape points to a transistor and contains the text: "and generate a selected one of a plurality of pump voltages (VHA2L)". Below the main circuit, there is a detailed schematic of a driver circuit labeled 'DRIVER 24' with inputs EN1, EN2, EN3 and outputs VP1, VP2. This driver circuit consists of multiple stages of transistors with various dimensions.</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.1 Voltage Switch 51</p>

Claim 1	Accused Product
	 <p>and generate a selected one of a plurality of pump voltages (VHA2L)</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4</p>

Claim 1	Accused Product
	 <p>and generate a selected one of a plurality of pump voltages (VHA_LDV2)</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2; Figure 7.3.14.5 Level Detector 6</p>

Claim 1	Accused Product
	 <p>and generate a selected one of a plurality of pump voltages (VHA_LDVPREF)</p>
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>

Claim 1

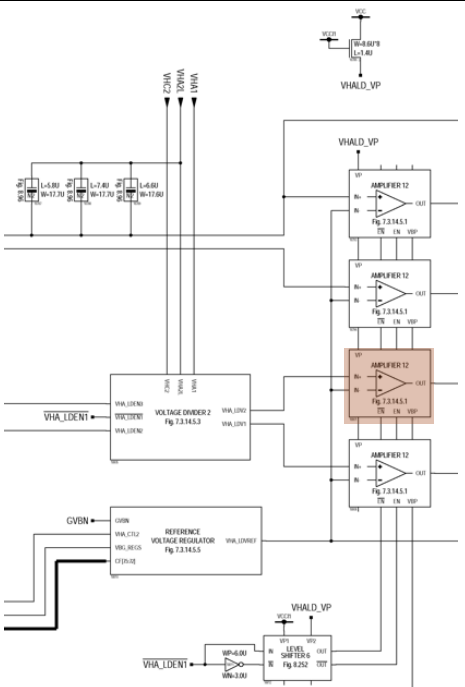
Accused Product

Figure 7.3.14.5.5 REFERENCE VOLTAGE REGULATOR

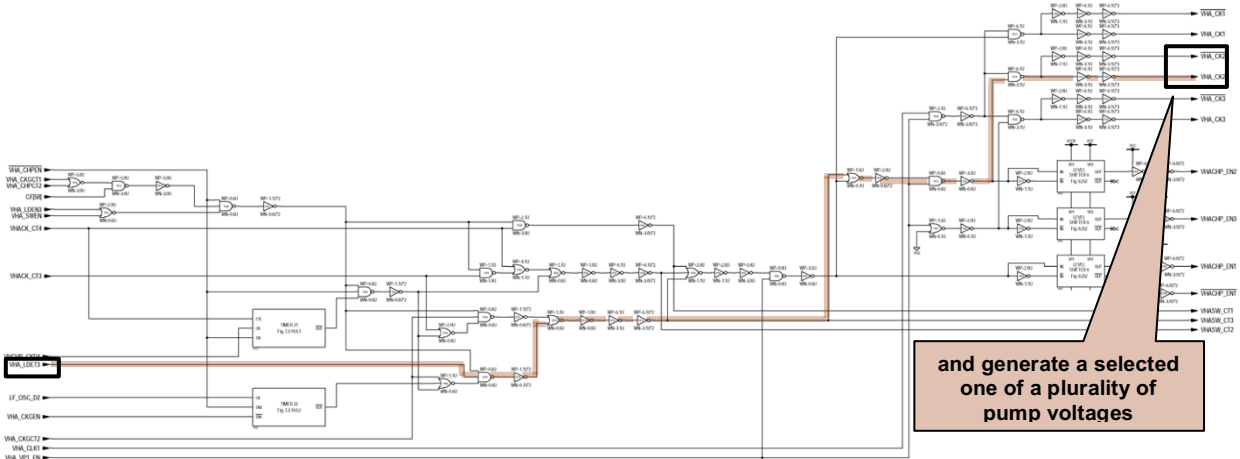
UNLESS OTHERWISE SPECIFIED THE SUBSTRATE BIAS OF ALL PMOS TRANSISTORS ARE CONNECTED TO VDD1
UNLESS OTHERWISE SPECIFIED THE SUBSTRATE BIAS OF ALL NMOS TRANSISTORS ARE CONNECTED TO VSS

Part #:	TOSHIBA 64L F1M1 256G		
DATE CODE:	NA	07/06/2015	201608
SCH NAME:	E_0003	DATE TIME:	10.10.2017.10:50
TECHINSIGHTS		VERSION: A	
WWW.TECHINSIGHTS.COM			

Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.5 Reference Voltage Regulator

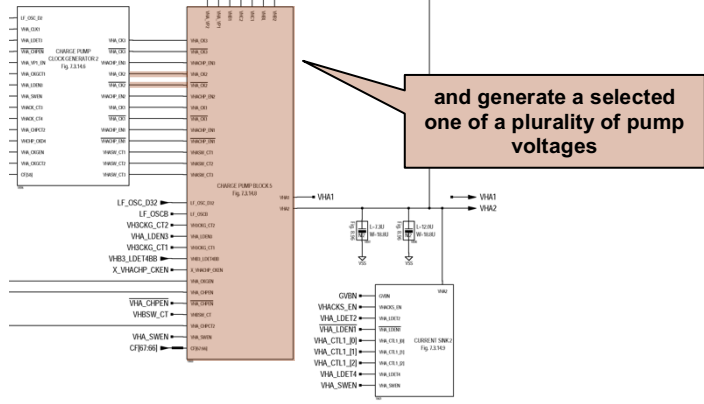
Claim 1	Accused Product
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>

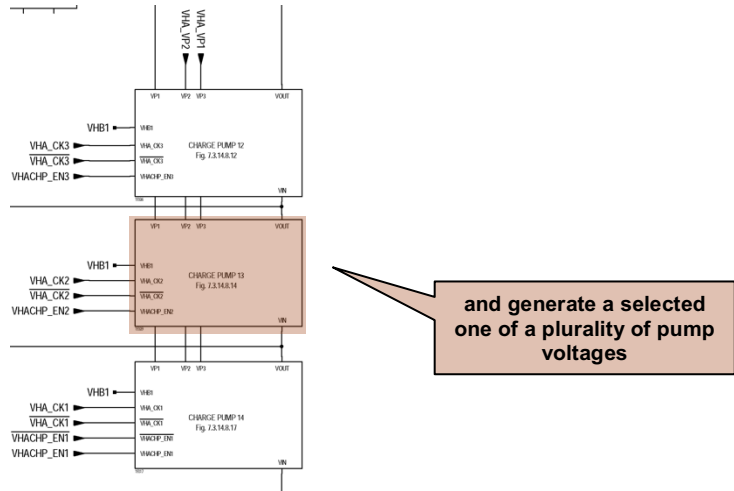
[illegible]

Claim 1	Accused Product
	<p data-bbox="646 272 940 365">VHA_LDET3 = 1 Disables VHA_CK2 pump clock to 1 level</p> <p data-bbox="1684 295 1843 354">VHA_CK2 = 1 VHA_CK2* = 0</p>  <p data-bbox="634 885 1831 954">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.6 Charge Pump Clock Generator 2</p>

Claim 1	Accused Product
	<p>and generate a selected one of a plurality of pump voltages</p>
	Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4

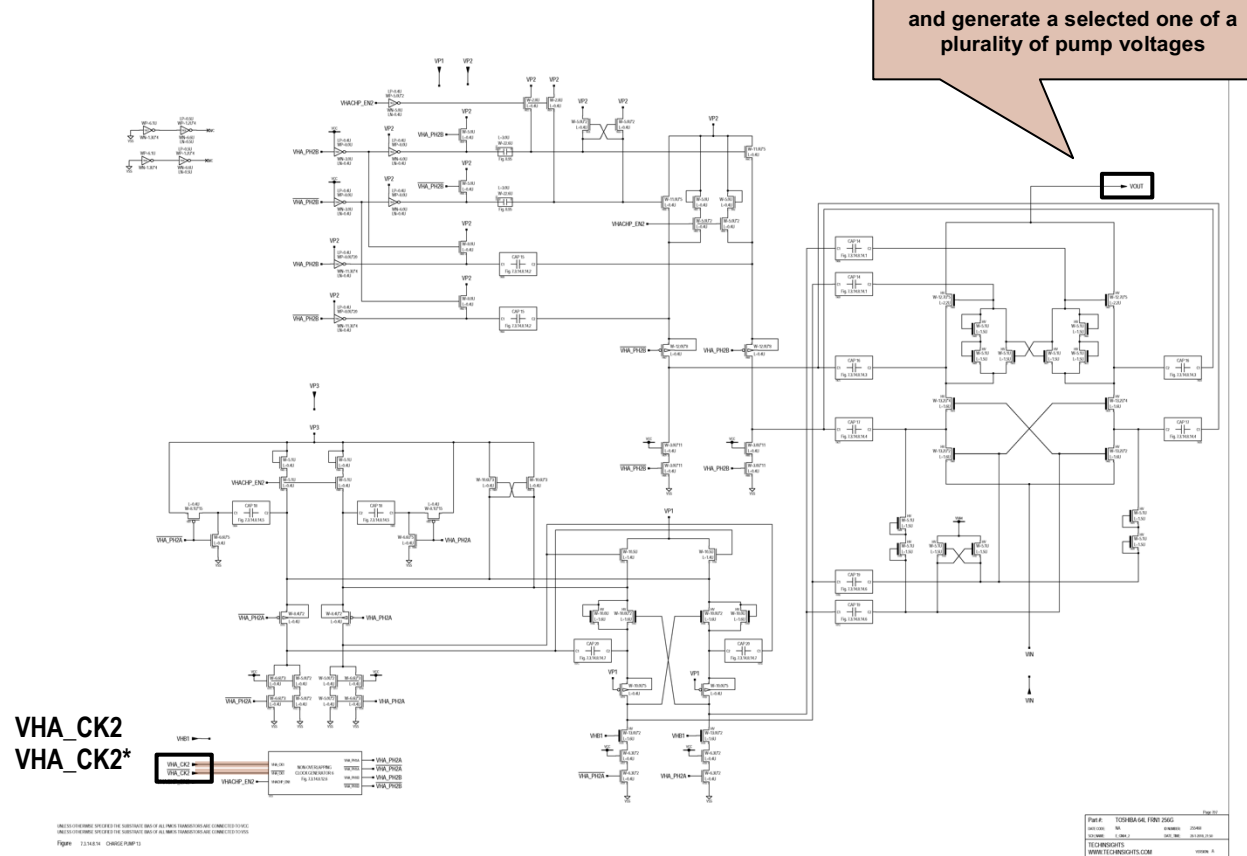
[illegible]

Claim 1	Accused Product
	 <p>and generate a selected one of a plurality of pump voltages</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4</p>

Claim 1	Accused Product
	 <p>The diagram illustrates a Charge Pump Block 5 containing three charge pumps: CHARGE PUMP 12 (Fig. 7.3.14.8.12), CHARGE PUMP 13 (Fig. 7.3.14.8.13), and CHARGE PUMP 14 (Fig. 7.3.14.8.14). Each pump has multiple input and output pins. A callout box points to the pumps with the text: "and generate a selected one of a plurality of pump voltages".</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5</p>

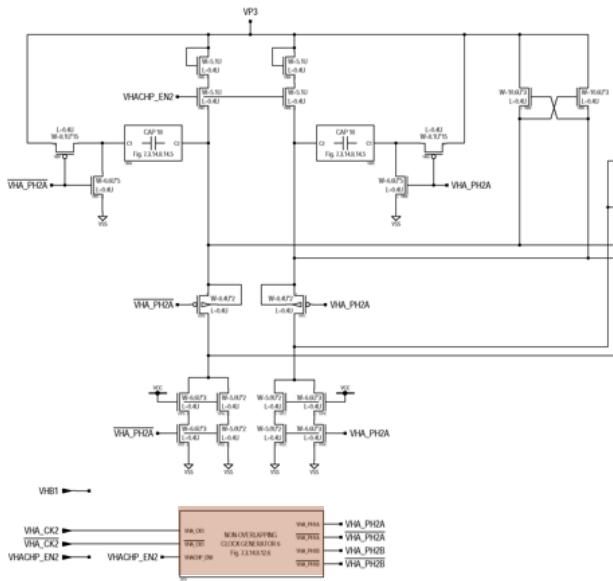
Claim 1

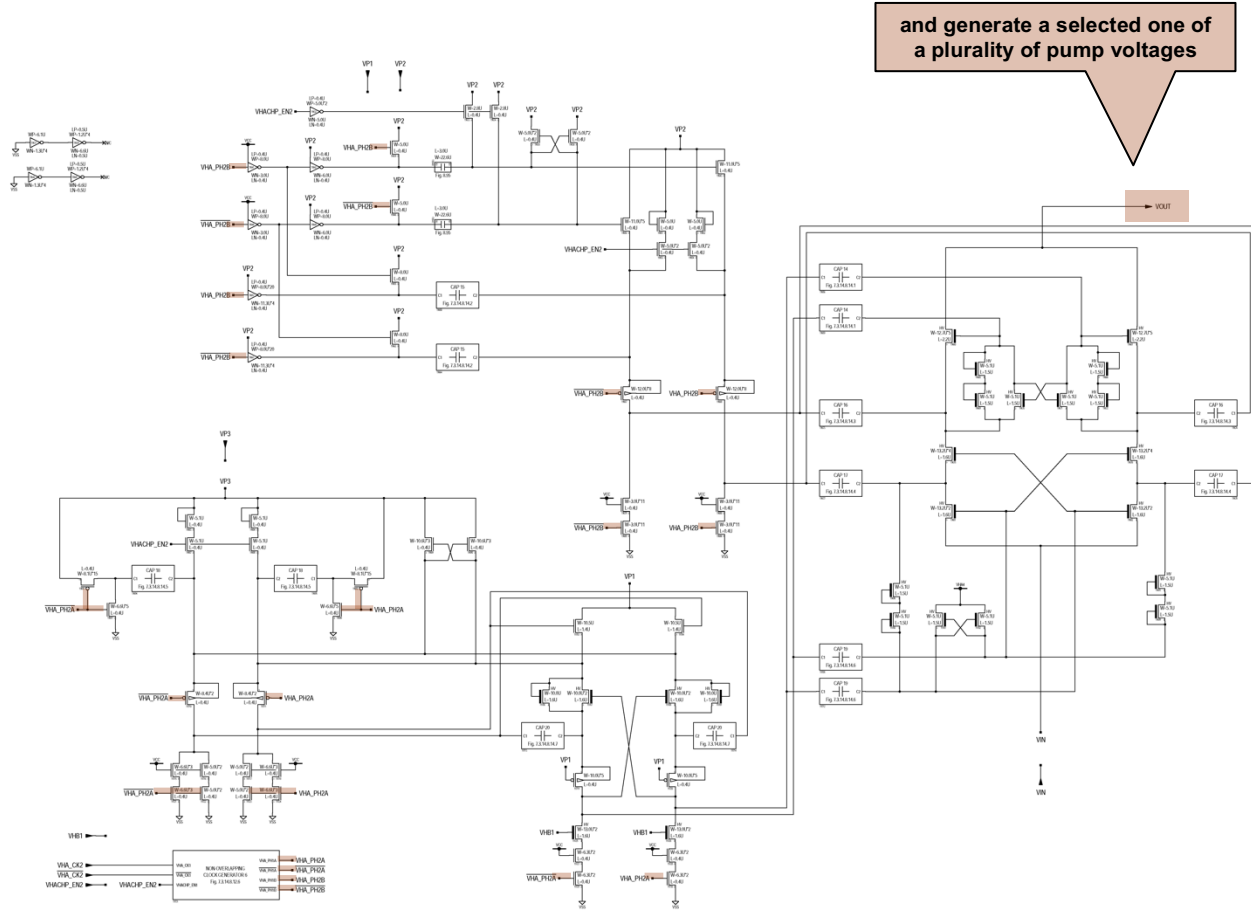
Accused Product



Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13

Claim 1	Accused Product
	<div style="text-align: right; margin-bottom: 10px;"> VHA_PH2A VHA_PH2A* VHA_PH2B VHA_PH2B* </div> <p style="margin-top: 20px;">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.12.6 Non-Overlapping Clock Generator 6</p>

Claim 1	Accused Product
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>

Claim 1	Accused Product
	 <p>and generate a selected one of a plurality of pump voltages</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>
1[b] a plurality of loads selectively coupleable to an output of the pumping circuit,	Each Accused Product includes a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage.

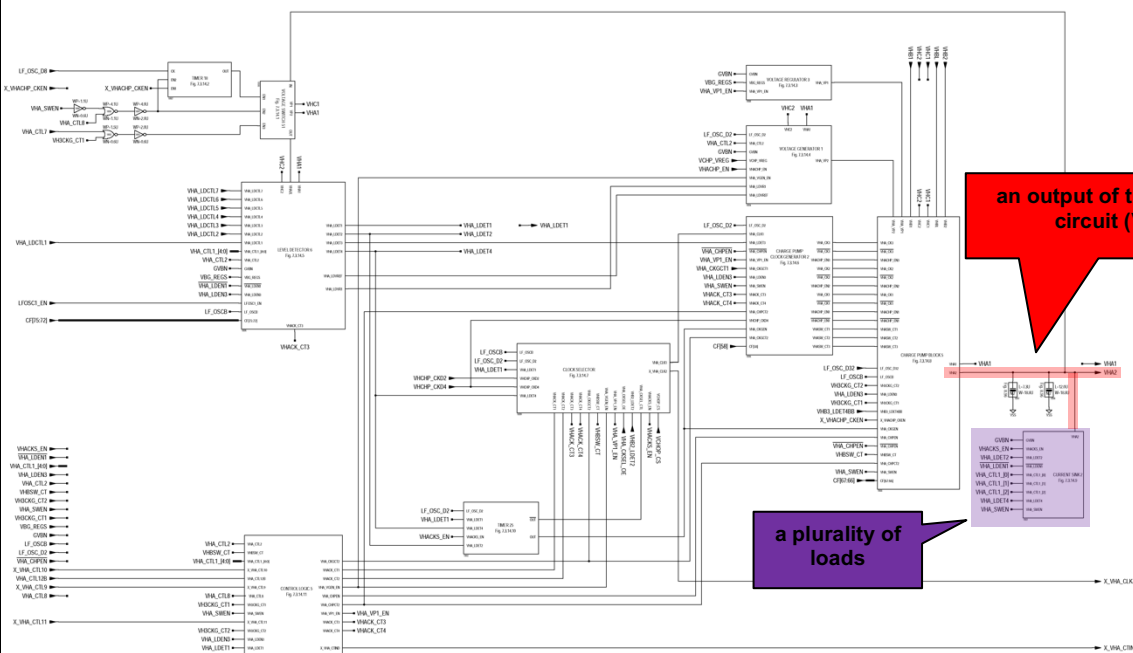
Claim 1

each load associated with a specific pump voltage; and

Accused Product

For example, VHA2 is an output of the pumping circuit. A plurality of loads (contained within Current Sink 2) can be selectively coupled to an output of the pumping circuit (for example VHA2). VHA2 is connected to pumping circuit output VHA1 through Voltage Switches 59 and 60. VHA1 is connected to wordline decoders during read or program operations. Read, program and erase operations require different voltages. Each load is associated with a specific pump voltage to carry out these functions.

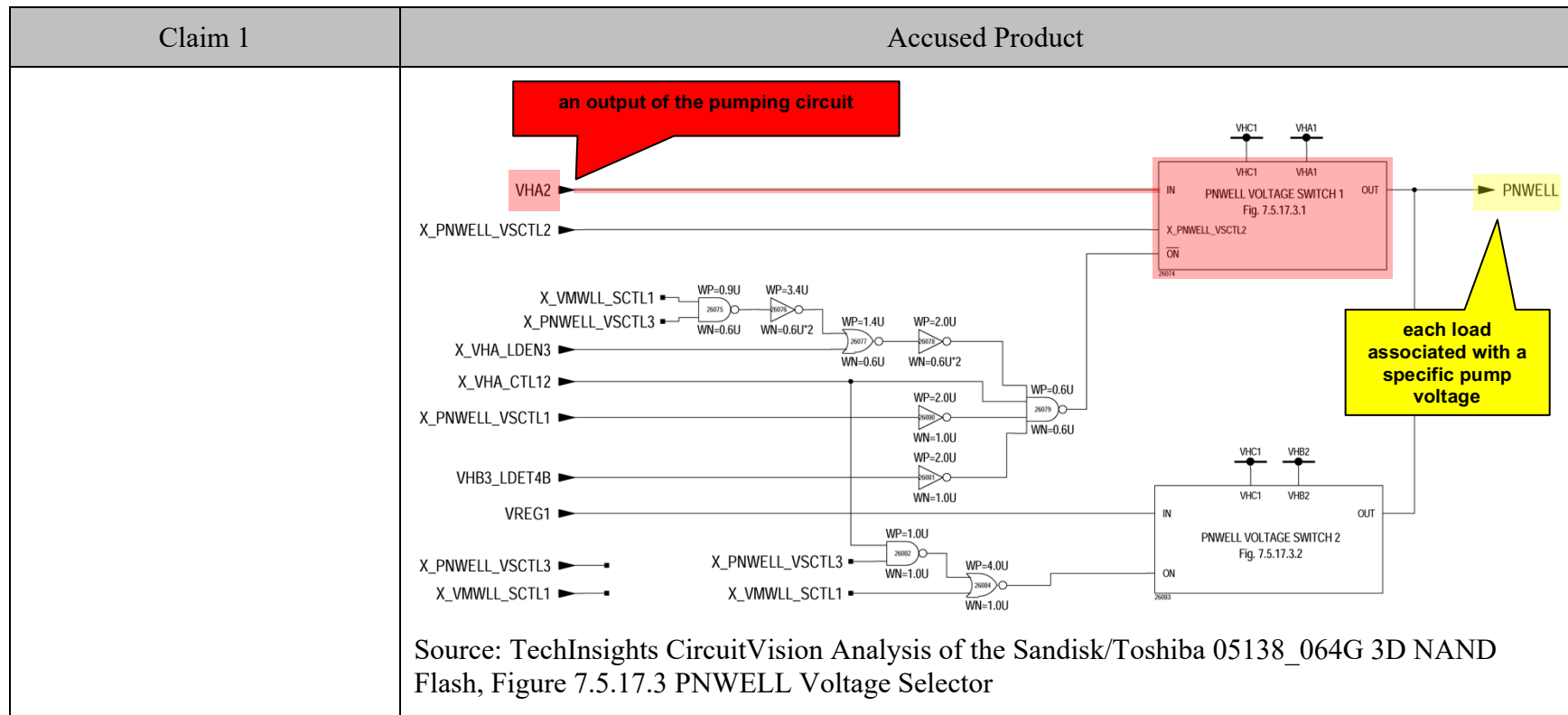
See, e.g.:

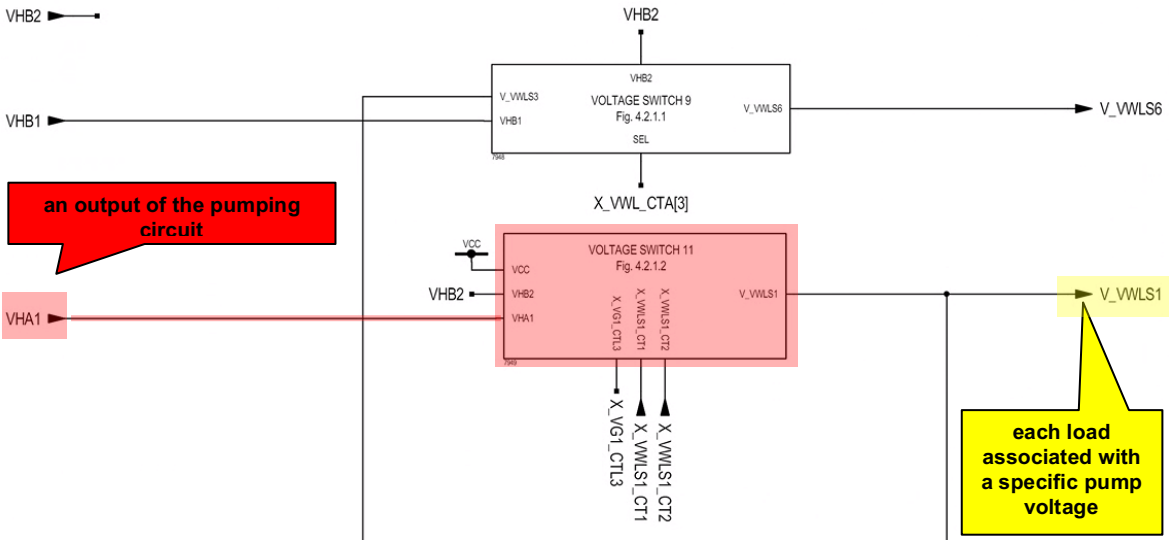


Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4

[illegible]

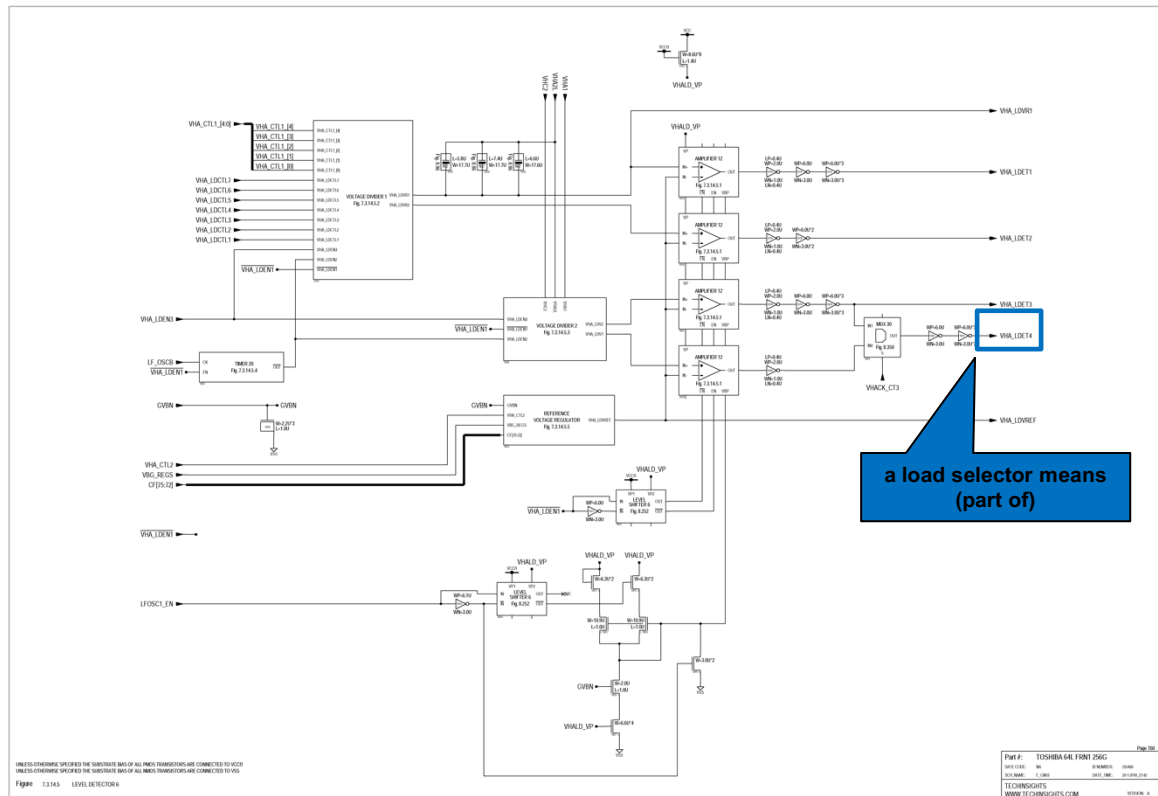
Claim 1	Accused Product
	<p>an output of the pumping circuit</p> <p>a plurality of loads</p> <p>selectively coupleable</p>
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p>



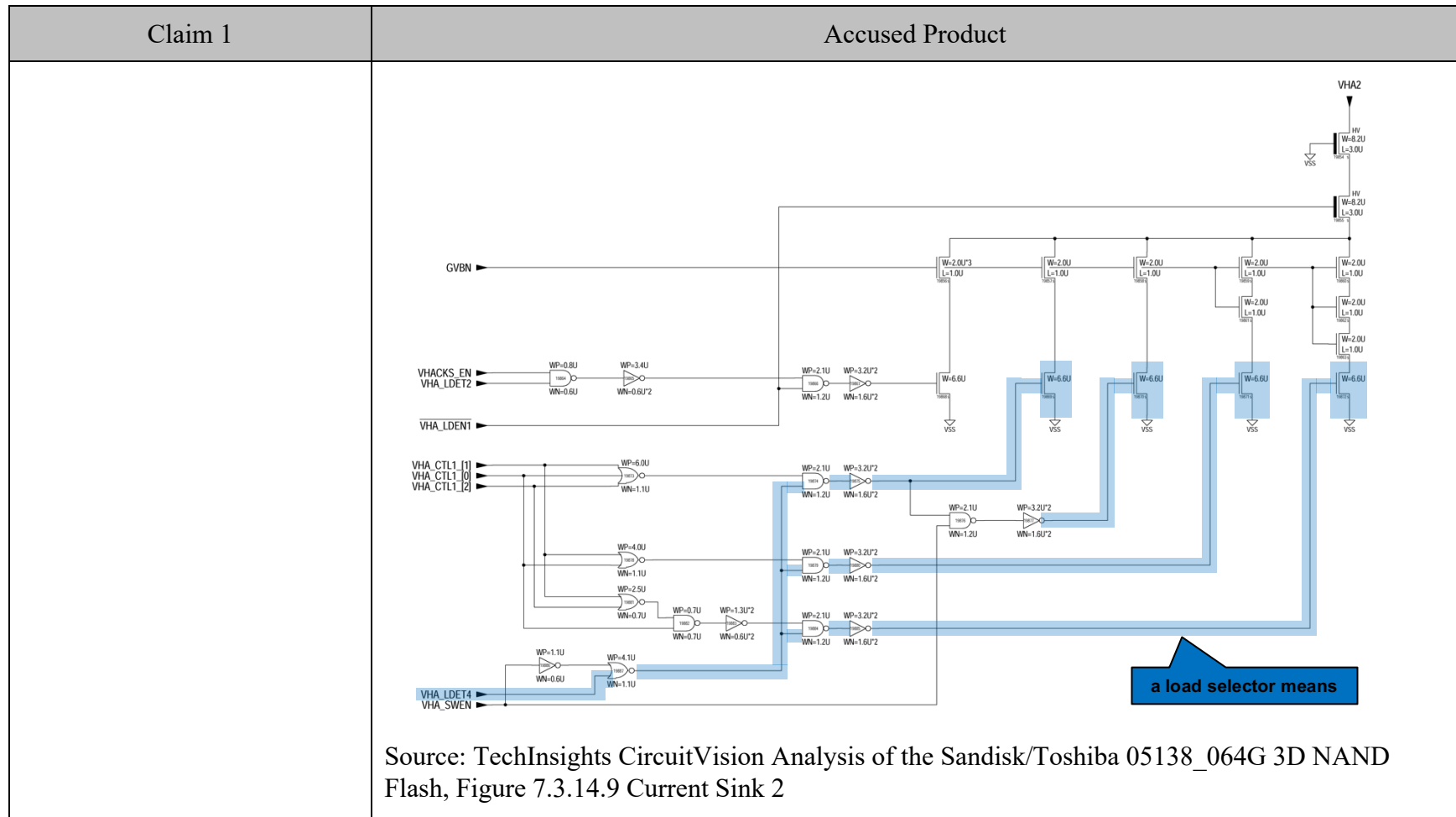
Claim 1	Accused Product
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 4.2.1 Wordline Voltage Switch Block 1</p>
<p>1[c] a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit</p>	<p>Each Accused Product includes a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.</p> <p>For example, the highlighted transistors below and their respective gate control signals form a load selector means. The output signal VHA_LDET4 from Level Detector 6 forms part of the load selector means. For example, the gate control signals are generated in part by a charge pump control signal (VHA_CTL1). This 3 bit value selectively couples a load associated with a specific pump voltage.</p> <p><i>See, e.g.:</i></p>

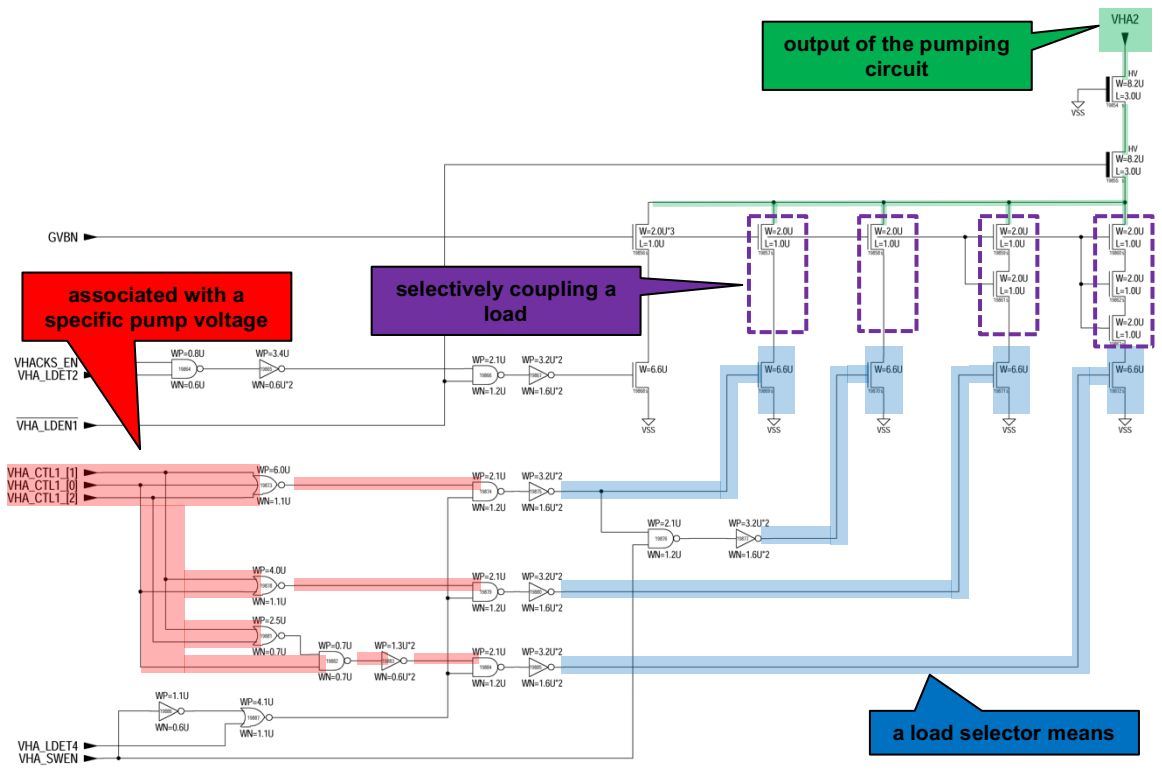
Claim 1

Accused Product



Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6



Claim 1	Accused Product
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p>

Claim 2

Claim 2	Accused Products
2. The charge pump circuit of claim 1, wherein the load selector means includes a	To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein the load selector means includes a target output pump selector for shutting down

Claim 2	Accused Products
<p>target output pump selector for shutting down the variable charge pump circuit when the target output pump voltage (Vcfra) is greater than or equal to a reference voltage (Vref).</p>	<p>the variable charge pump circuit when the target output pump voltage (Vcfra) is greater than or equal to a reference voltage (Vref).</p> <p>For example, VHA2 is provided to a level detector which suspends pump clocks when a desired level is reached. VHA2 is scaled by a fixed ratio voltage divider (Voltage Divider 2). It is then compared (using Amplifier 12) to an adjustable reference voltage (generated by Reference Voltage Regulator). A 4-bit digital code CF(75:72) adjusts the output reference voltage by shorting out resistors in a resistor divider, thereby providing programmable pump output voltage levels on VHA1 and VHA2. A comparator (Amplifier 12) compares the scaled VHA2 to the programmable reference voltage. If the scaled VHA2 exceeds the programmable reference voltage, output VHA_LDET3 transitions from 1 to 0 to stop further pumping.</p> <p><i>See evidence and explanation for claim element [1a], supra.</i></p>

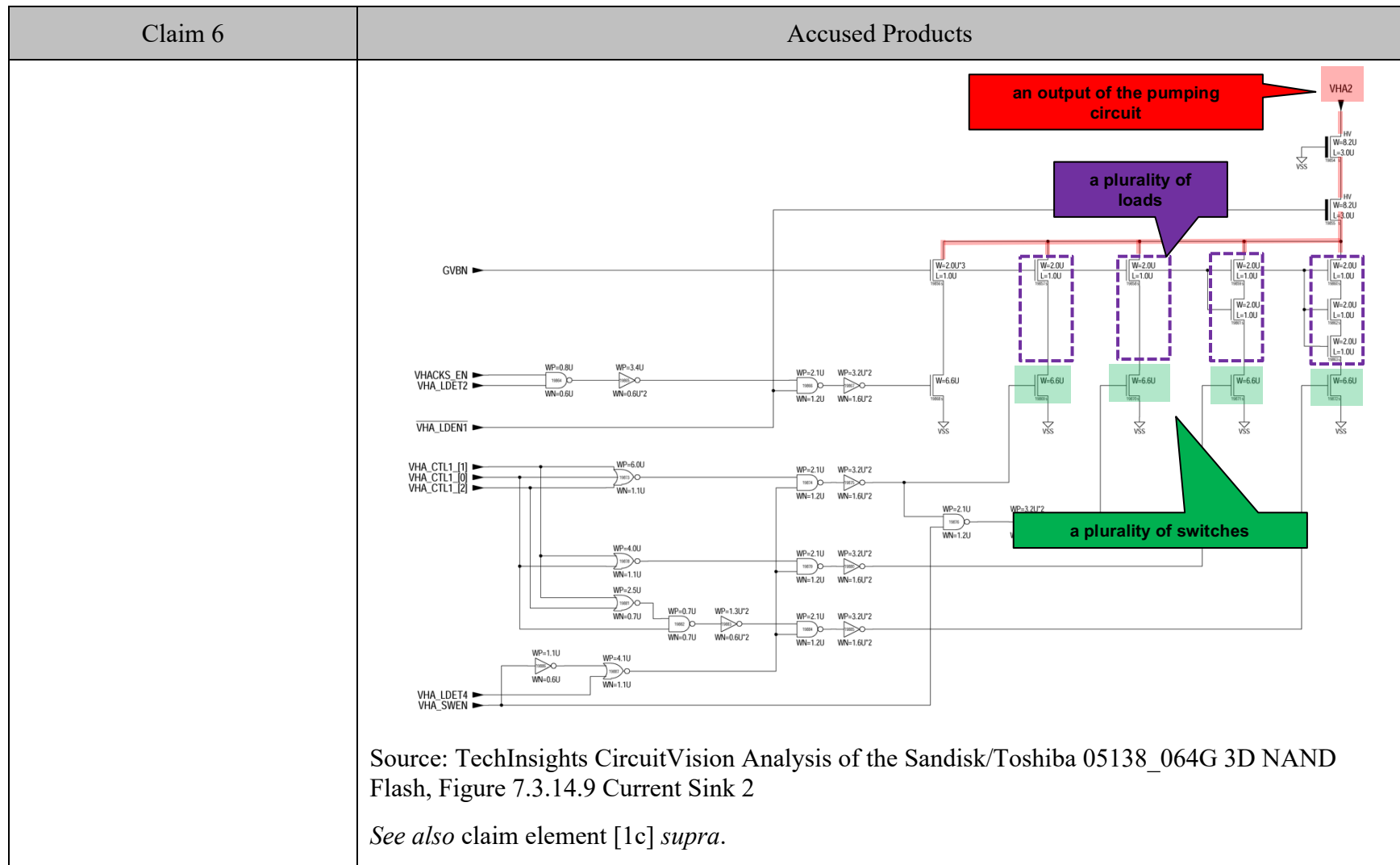
Claim 3

Claim 3	Accused Products
<p>3. The charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, whenever a maximum ripple on the target output voltage (Vcfrb) greater than the reference voltage (Vref) then the maximum ripple on the target output selector means adds additional loads until the Vcfrb voltage is</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, and whenever a maximum ripple on the target output voltage (Vcfrb) greater than the reference voltage (Vref) then the maximum ripple on the target output selector means adds additional loads until the Vcfrb voltage is less than or equal to the reference voltage (Vref).</p> <p><i>See evidence and explanation for claim element [1a] and claim 2, supra.</i></p>

Claim 3	Accused Products
less than or equal to the reference voltage (V_{ref}).	

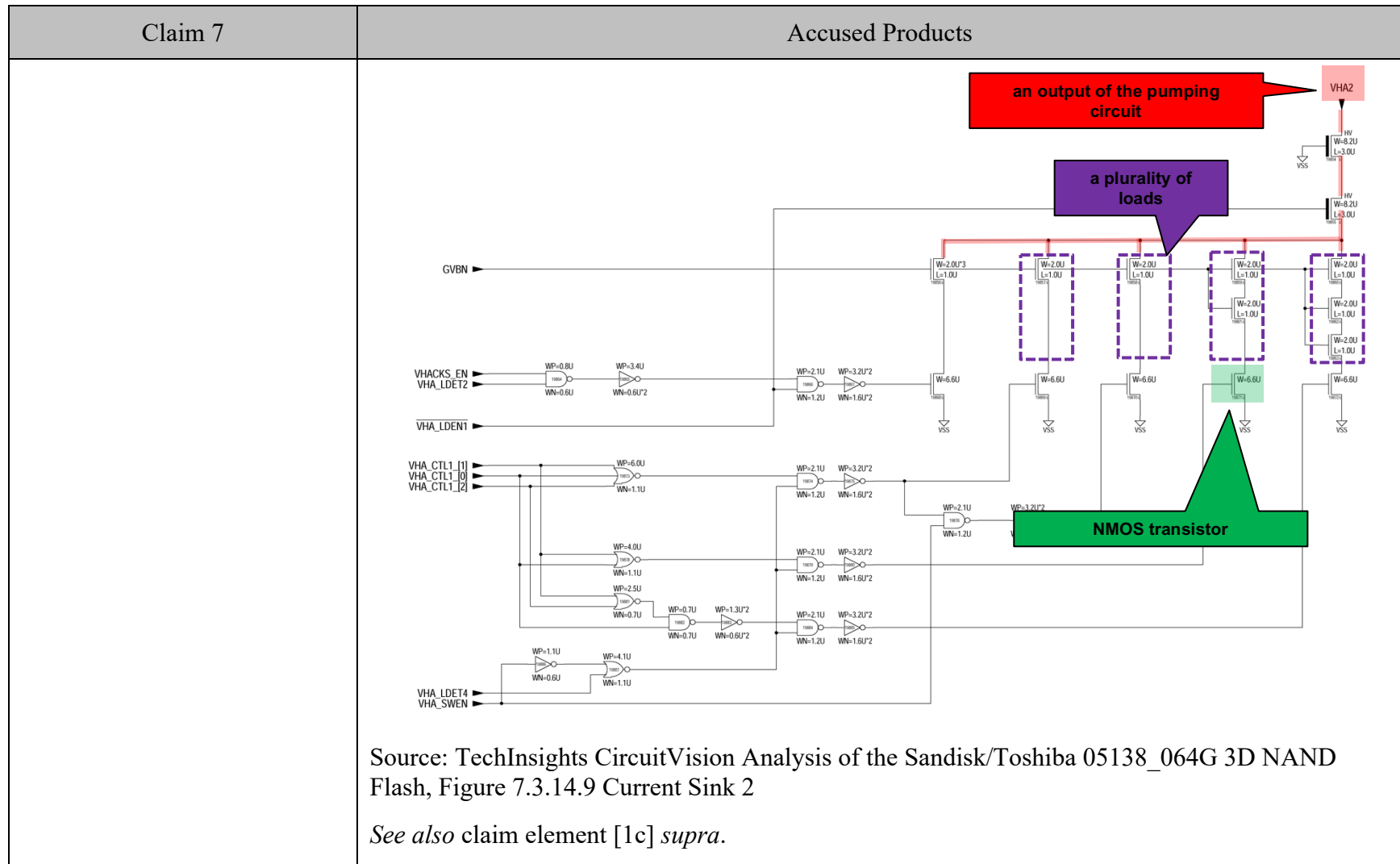
Claim 6

Claim 6	Accused Products
6. The charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.</p> <p><i>See, e.g.:</i></p>



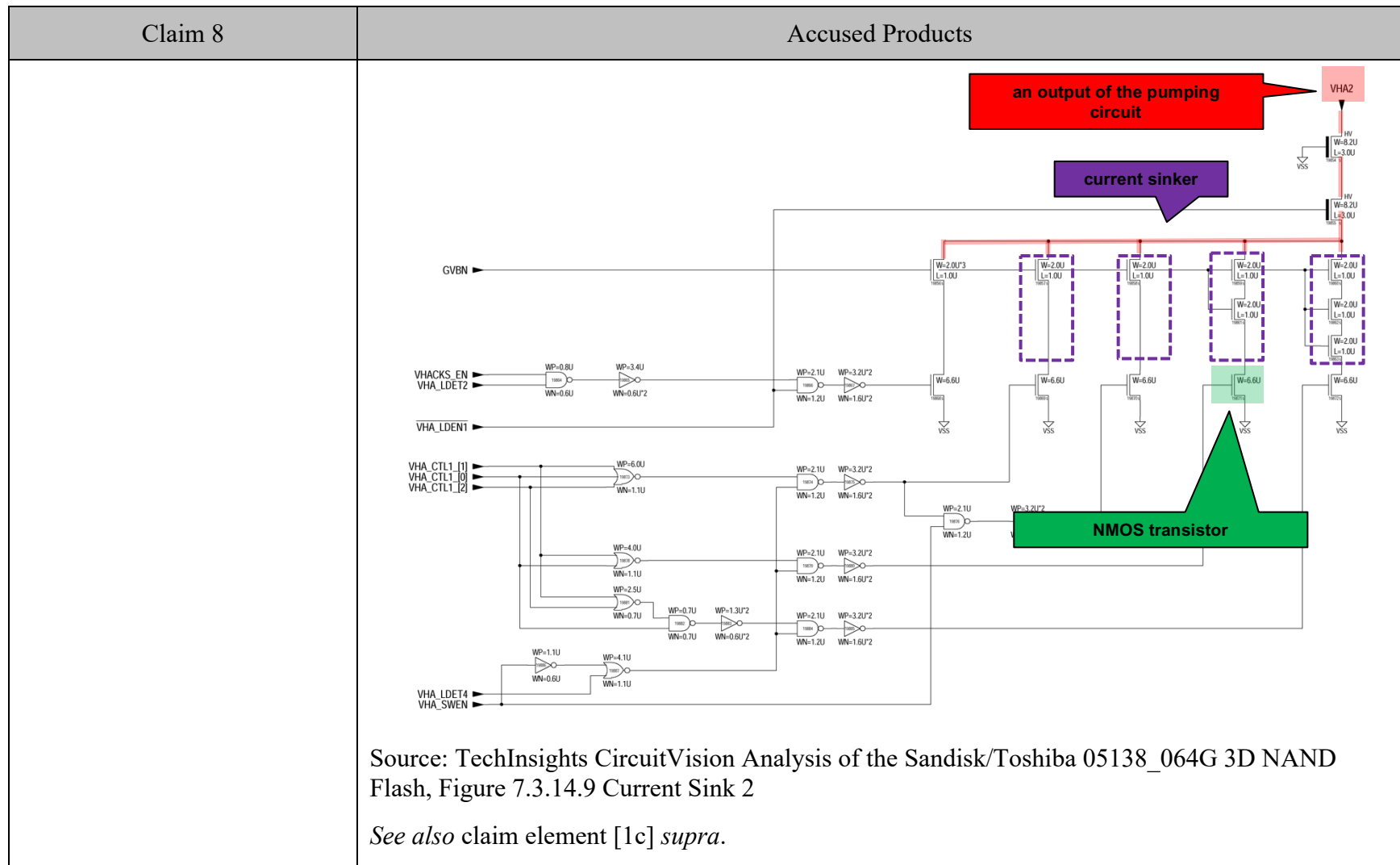
Claim 7

Claim 7	Accused Products
<p>7. The charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.</p> <p><i>See, e.g.:</i></p>



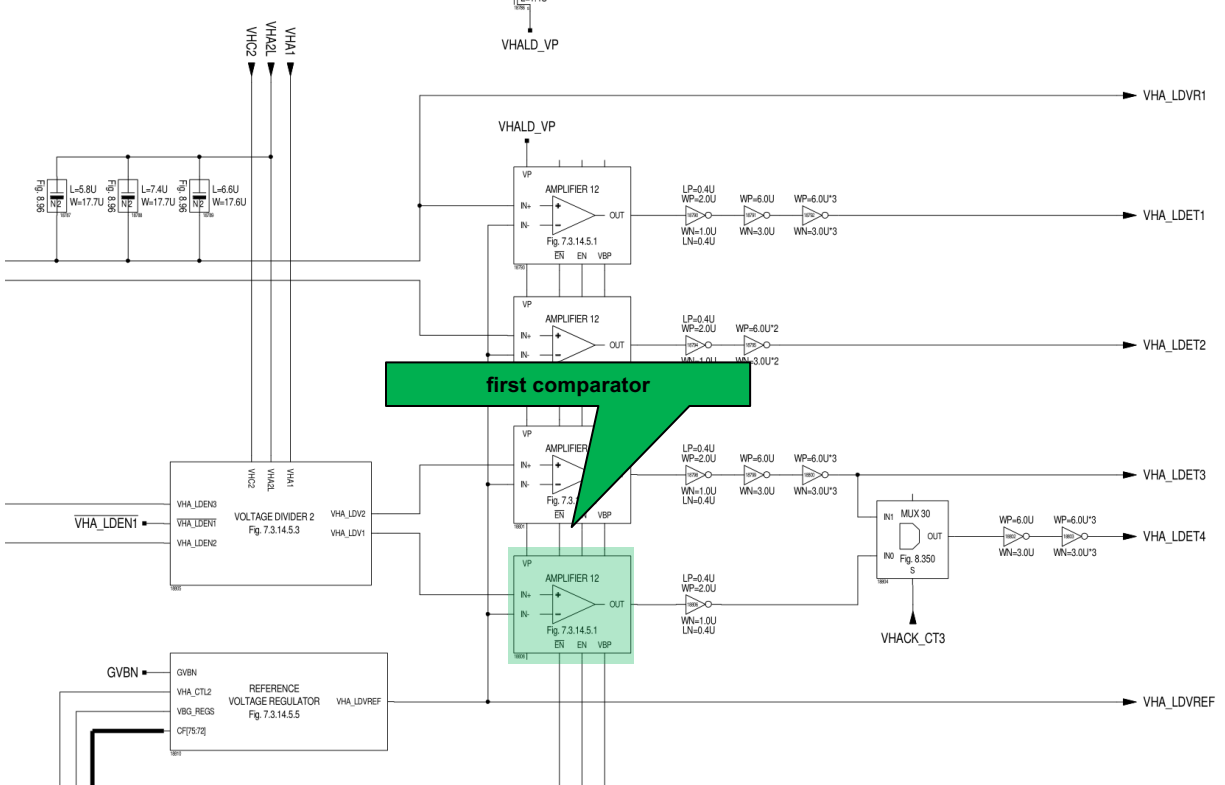
Claim 8

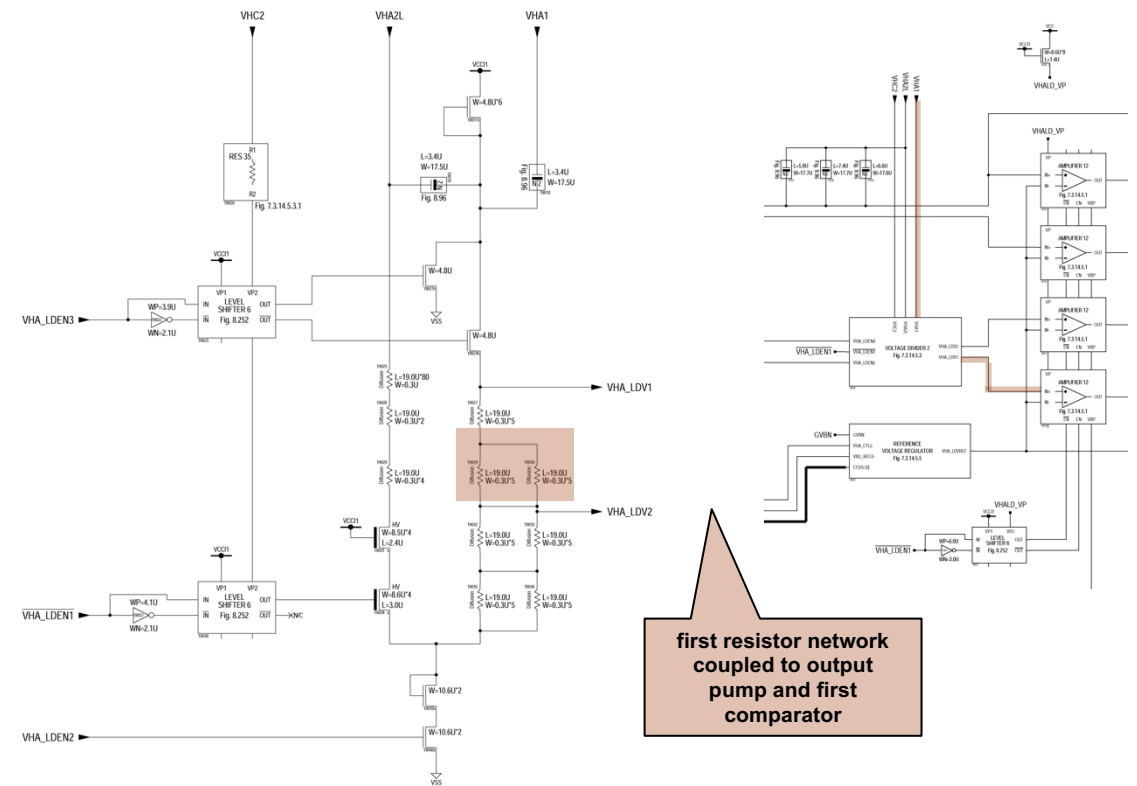
Claim 8	Accused Products
<p>8. The charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.</p> <p><i>See, e.g.:</i></p>

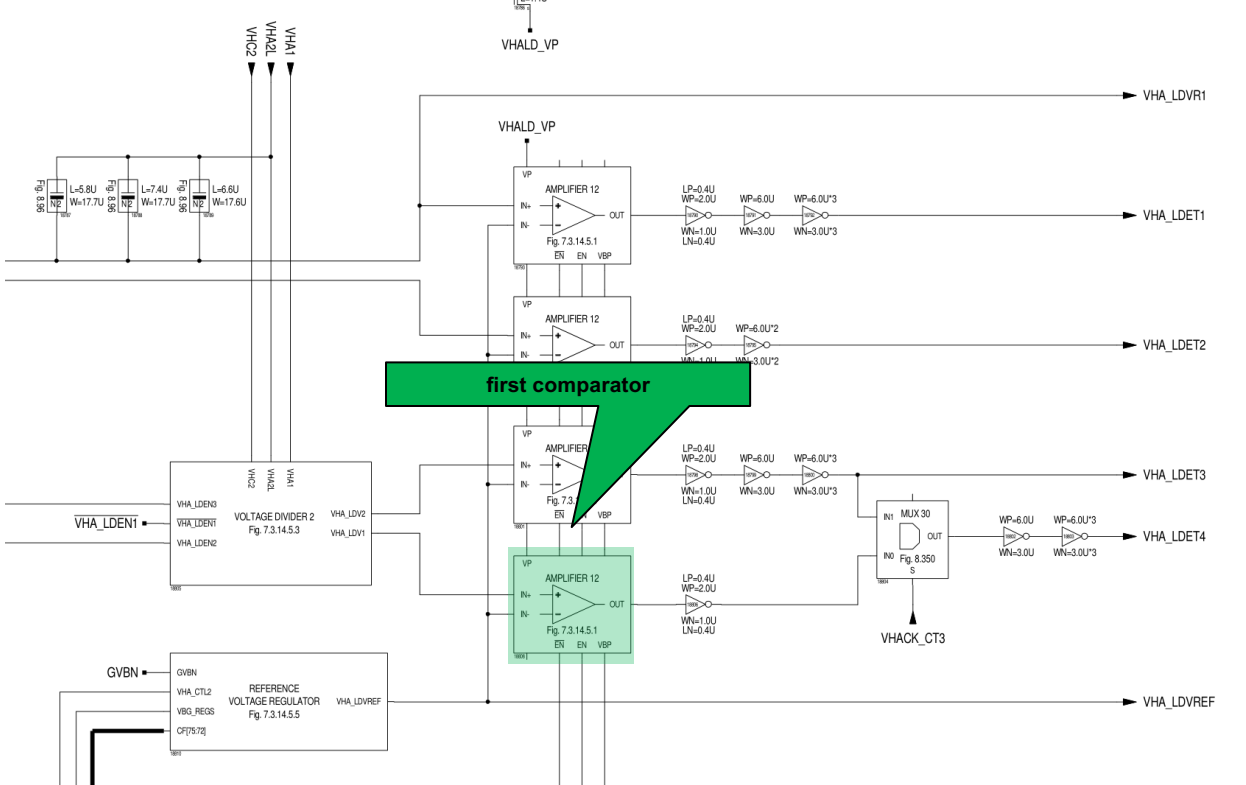


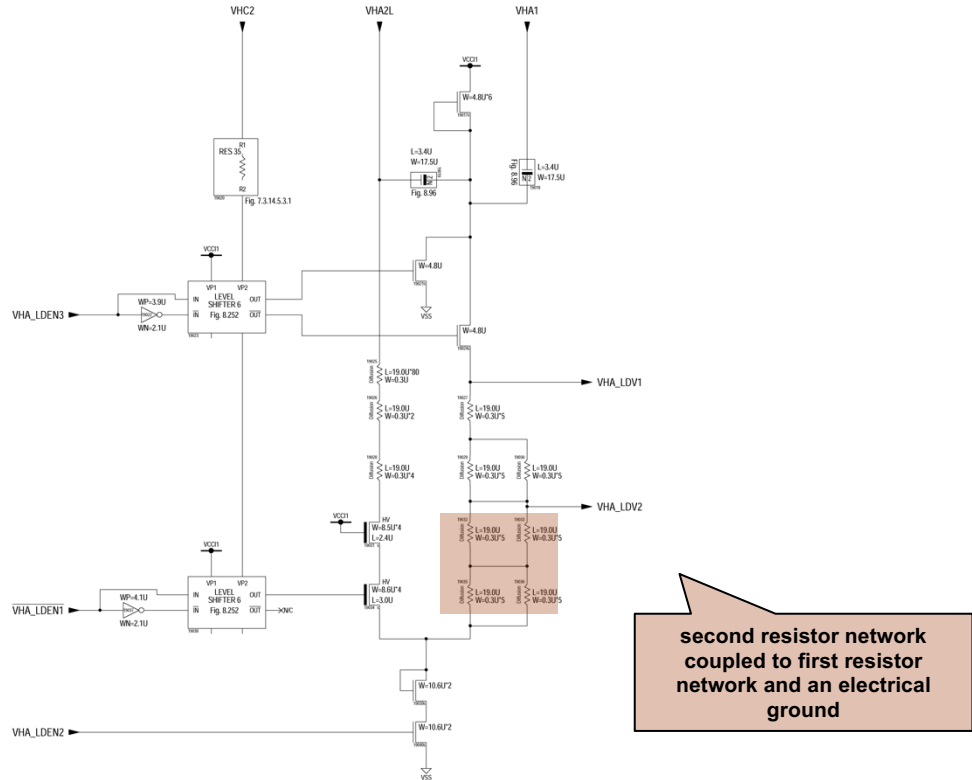
Claim 11

Claim 11	Accused Products
[11pre] 11. The charge pump circuit of claim 2 wherein the target output pump selector comprises:	Each Accused Product includes the charge pump circuit of claim 2. <i>See supra</i> claim 2.
[11a] a) a first comparator having two input terminals, an output terminal and a first enable terminal, one of the two input terminals being connected to the reference voltage (Vref);	Each Accused Product includes a first comparator having two input terminals, an output terminal and a first enable terminal, one of the two input terminals being connected to the reference voltage (Vref). <i>See, e.g.:</i>

Claim 11	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>
<p>[11b] b) a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to one of the input terminals of the first comparator;</p>	<p>Each Accused Product includes a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to one of the input terminals of the first comparator.</p> <p><i>See, e.g.:</i></p>

Claim 11	Accused Products
	 <p>The image displays two circuit diagrams from a patent document. The left diagram, labeled 'Fig. 7.3.14.5.1', is a voltage divider circuit with inputs VHC2, VHA2L, and VHA1. It features a resistor network (RES 35) and a level detector (LEVEL SHIFTER 6) with inputs VHA_LDEN3 and VHA_LDEN1. The right diagram, labeled 'Fig. 7.3.14.5.2', is a level detector circuit with inputs VHA_LDEN1 and VHA_LDEN2. It includes a voltage divider (VIA_DIVIDER 2) and a level detector (LEVEL SHIFTER 6). A callout box points to a resistor network in the level detector circuit, stating: 'first resistor network coupled to output pump and first comparator'.</p>
<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2; Figure 7.3.14.5 Level Detector 6</p>	

Claim 11	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>
<p>[11c] c) a second resistor network having two terminals, the first terminal being coupled to the second terminal of the first resistor network, and the second terminal of the second resistor network being</p>	<p>Each Accused Product includes a second resistor network having two terminals, the first terminal being coupled to the second terminal of the first resistor network, and the second terminal of the second resistor network being coupled to an electrical ground.</p> <p><i>See, e.g.:</i></p>

Claim 11	Accused Products
coupled to an electrical ground; and	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2</p>
[11d] d) a reference voltage source (Vref) coupled to one of the input terminals of the first comparator.	<p>Each Accused Product includes a reference voltage source (Vref) coupled to one of the input terminals of the first comparator.</p> <p><i>See, e.g.:</i></p>

Claim 11	Accused Products
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>